Notice of Allowability	Application No. 09/471,675	Applicant(s) ANDERSON ET AL.	
	Examiner Thomas Heckler	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are *1-28*.
3. ☒ The drawings filed on *24 December 1999* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☒ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. _____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (PTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No._____.
5☒ Information Disclosure Statements (PTO-1449), Paper No. *2-4*.
6☒ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

Thomas Heckler
Primary Examiner
Art Unit: 2185

1. The following changes to the drawings are required by the examiner: labels are required for the boxes of Figs. 1, 3, 4 as per 37 C.F.R. 1.83(a). In order to avoid abandonment of the application, applicant must make these drawing changes.

2. The following is an examiner's statement of reasons for allowance: the prior art does not teach a processing mechanism for processing unprocessed micro devices into processed micro devices comprising a pin driver module for routing address, data and control signals to a backplane module and provide a first plurality of voltages to the backplane module, the backplane module routing the address, data and control signals and providing a second plurality of voltages to at least one socket wherein the unprocessed micro device is placed;

nor does the prior art teach a buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices comprising a digital-to-analog converter to generate a first variable DC voltage, an amplifier responsive to the DC voltage to generate a second variable DC voltage, and a level-shifting translating buffer for transferring data signals from a processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor, the buffer responsive to a voltage and the second variable DC voltage to provide a plurality of logic levels for the device data signals;

nor does the prior art teach a method for programming a programmable micro device comprising providing a first address from a processor, providing a first data corresponding to the

first address, and providing a control signal to enable the micro device to accept the data at a memory location identified by the first address;

nor does the prior art teach a method for reading a programmable micro device comprising providing a first address from a processor to the micro device and providing a control signal from the processor to the micro device to enable the device to provide a first data from a memory location identified by the first address;

nor does the prior art teach a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices comprising a plurality of sockets for placement of processed micro devices, a plurality of data buffer/registers, each coupled to a socket for receiving a first data, a plurality of compare circuits having one input coupled to a respective buffer/register, an expected data register coupled to the second input of a respective compare circuit, and a processor coupled to the output of each of the plurality of compare circuits, wherein each compare circuit provides a first logic level when the first data matches the first expected data, and provides a second logic level when the first data does not match the first expected data;

nor does the prior art teach a method for verifying data programmed in a plurality of programmed micro devices comprising providing to each of a plurality of data buffer/registers a first data stored in each of the plurality of programmed micro devices, providing the first data to a first input of a plurality of compare circuits, providing a first expected data from an expected data register to a second input of each of the plurality of compare circuits, comparing the first data

with the first expected data, outputting a first logic level from one of the compare circuits when the first data matches with the first expected data, and outputting a second logic level from one of the compare circuits when the first data does not match with the first expected data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Heckler whose telephone number is (703) 305-9666.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 305-3900.

THOMAS M. HECKLER
PRIMARY EXAMINER

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November 5, 2002